

## **REMARKS / ARGUMENTS**

The Office Action mailed October 10, 2006 has been reviewed. The Applicants' attorney appreciates the Examiner citing MPEP § 2113 which states "PRODUCT-BY-PROCESS CLAIMS ARE NOT LIMITED TO THE MANIPULATIONS OF THE RECITED STEPS, ONLY THE STRUCTURE IMPLIED BY THE STEPS." In this case, several structural differences between claims 1, 25 and the Patel et al. reference were discussed in the response filed on July 19, 2006. For example, it was discussed that Patel does not teach areas of thick conductive material forming a predetermined pattern of conductor traces extending laterally on the thin base. It was also discussed that Patel does not teach areas of thick conductive material that are covered by the sublayer, see for example the Interview Summary dated January 17, 2006:

The applicant(s) explained differences between the claimed invention and the prior art. The applicant(s) proposed a future amendment for discussion that included the feature of the sublayer covering the areas of thick conductive material. The examiner noted that the addition of this feature to claim 1 and 25 would appear to overcome the prior art. The applicant(s) noted that they would file a subsequent response formally for consideration.

In an effort to expedite the allowance of claims 1-4, 6-12 and 25-35, such claims have been amended to be in a process format, rather than a product by process format. For the reasons set forth below, Applicants believe claims 1-4, 6-12, and 25-35 are in condition for allowance.

**Rejection of Claims 1-3, 6-8, 25-27, and 31 Under 35 U.S.C. § 102(e)**

In the Office Action mailed March 30, 2006 (which was incorporated by reference in the Office Action mailed October 10, 2006), the Examiner rejected Applicants' claims 1-3, 6-8, 25-27, and 31 under 35 U.S.C. § 102 as being anticipated by Patel et al. (US 6,623,651).

As set forth below, Applicants respectfully submit that the rejection of claims 1-3, 6-8, 25-27, and 31 under 35 U.S.C. § 102 is overcome for the reason that the Patel reference does not disclose, teach, or even suggest the invention recited in Applicants claims 1-3, 6-8, 25-27, and 31.

The Patel reference is directed to "a method for making a multi-layer electrical circuit board having at least one electrically conductive portion or "via" which traverses through the multi-layer electrical circuit board (See Patel, Col. 1, lines 10-14. In contrast, Applicants' invention is directed to a method of producing a printed circuit board having a single layer containing both thin conductor areas for fine resolution conductors and thick conductor areas for power circuits (See Pedretti, Paragraph 17 for example).

As the Examiner is aware, a rejection under 35 U.S.C. § 102(e) requires each and every element of the claimed invention to be taught in a single prior art reference. The Examiner asserts that the Patel reference teaches a printed circuit board comprising: a conductor core containing a thin base of electrically conductive material and areas of thick conductive material; a sublayer of electrically insulating material to create a flat laminate wherein the areas of thick conductive material are positioned adjacent to and covered by the sub-layer; and

predetermined printed circuits having both thick conductor traces formed from the thick conductive material and fine resolution traces from the thin base. The Office Action refers solely to figure 1M of the Patel reference to support these statements.

When Figure 1M is examined in the context of the entire patent, it is apparent that the cross-section depicted in Figure 1M is quite different from Applicants' invention. Applicants respectfully disagree that all elements listed in the office action are disclosed by Patel. Applicants further submit that all elements of claim 1 are not taught by Patel.

Applicants claim 1 recites a process for making a printed circuit board comprising the steps of:

forming a conductor core containing a thin base of electrically conductive material and areas of thick conductive material, the thick conductive material in a predetermined pattern of conductor traces extending laterally on the thin base;

bonding the conductor core to a sublayer of electrically insulating material to create a flat laminate, wherein the areas of thick conductive material are positioned adjacent to and are covered by the sublayer; and,

forming predetermined printed circuits having both thick conductor traces formed from the thick conductive material and fine resolution traces formed from the thin base by removing conductive material from the

flat laminate that does not comprise said predetermined printed circuits to form the predetermined printed circuits.

Applicants' claim 1 recites several unique elements that are not taught by the Patel reference. First, Applicants respectfully submit that Patel does not teach areas of thick conductive material forming a predetermined pattern of conductor traces extending laterally on the thin base. Rather, the Patel reference teaches "selectively creating . . . several nubs, bumps, or protuberances" (See Patel, Col. 1, lines 55-56). The contextual meaning of nubs, bumps, or protuberances is made clear in numerous places within the Patel reference:

"multi-layer electrical circuit having at least one electrically conductive portion or 'via' which traverses through the multi-layer electrical circuit board" (See Patel, Col. 1, lines 10-14)

"multi-layer circuit assembly having an interconnection portion which extends through the formed multi-layer circuit" (See Patel, Col. 2, lines 63-65)

"thereby forming the a multi-layer circuit board and causing the at least one protuberance to extend through the multi-layer circuit board" (See Patel, Col. 3, lines 10-13)

"thereby creating a multi-layer circuit assembly while causing the at least one protuberance to interconnectingly extend through the multi-layer circuit assembly (See Patel, Col. 3, lines 19-22)

"It should be understood that the multi-layer circuit board and/or assembly includes electrically conductive 'vias' or interconnection portions, such as portion 100, which traverse the multi-layer electrical circuit board 98, and which allows the various layers or members 12, 34, 56, 58, 80, and 82 to be electrically interconnected. Each interconnection portion, such as portion 100, thereby extends a unique one of each protuberances 15 through the formed multi-layer circuit assembly 98 while obviating the need to drill and/or electroplate a formed aperture." (See Patel, Col. 6, lines 19-28)

Thus, the Patel reference makes clear that the nubs, bumps, or protuberances extend perpendicularly from the conductive member 12 at discrete

points to electrically interconnect the various layers of a multi-layer circuit, rather than defining a "predetermined pattern of conductor traces extending laterally on the thin base," as recited in Applicants' claim 1.

Secondly, the Office Action states that the Patel reference teaches "the areas of thick conductive material are positioned adjacent to and covered by the sublayer." Applicants respectfully disagree. As depicted in the manufacturing step shown in figure 1C of Patel, "a certain substance or material 22 is applied upon member 12 and substantially 'fills' depressed portions 18" (See Patel, Col. 3, lines 62-63). As shown, the material only fills the depressed portions, leaving the protuberances of conductive material exposed for contact with further layers of conductive materials. Thus, Patel does not teach areas of thick conductive material that are covered by the sublayer.

Applicants' independent claim 25 is similar to claim 1, except that claim 25 is directed to a process for making a printed circuit core suitable for use as a component of a multilayer printed circuit board. The above remarks regarding claim 1 will not be repeated, but are deemed relevant to the rejection of claim 25 and are expressly incorporated herein by reference. Although suitable for use in a multilayer printed circuit, Applicant's claim 25 contains the same features of claim 1 that distinguish it from the Patel reference. Thus, Patel does not teach the inventive concept recited in Applicants' claim 25.

It should be noted that claims 2-3 and 6-8 depend upon claim 1 and that claims 26-27 and 31 depend upon claim 25, and thus contain every limitation of claims 1 and 25, respectively. Thus, no further comments concerning claims 2-3,

6-8, 26-27, and 31 are deemed necessary herein to be fully responsive to the Office Action dated October 10, 2006.

In light of the foregoing, it is Applicants' belief that claims 1-3, 6-8, 25-27, and 31 are patentable under 35 U.S.C. § 102(e) in view of Patel. Therefore, reconsideration and withdrawal of the rejection of claims 1-3, 6-8, 25-27, and 31 is respectfully requested.

**Rejection of Claims 4, 9-12, 28-30, and 32-35 Under 35 U.S.C. §103(a)**

Claims 4, 9-12, 28-30 and 32-35 were also rejected under 35 USC 103(a) as being unpatentable over Patel et al. (US 6,623,651) in view of Bokisa (US 5,928,790). As the Examiner is aware, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestions to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F. 2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

As discussed above, the Patel reference does not teach or disclose areas of thick conductive material forming a predetermined pattern of conductor traces extending laterally on the thin base. Rather, the Patel reference teaches

“selectively creating . . . several nubs, bumps, or protuberances” (See Patel, Col. 1, lines 55-56). Further, Patel is focused solely on “at least one electrically conductive portion or ‘via’ which traverses through the multi-layer electrical circuit board” (See Patel, Col. 1, lines 11-14). The Patel reference contains no suggestion that areas of thick conductive material could be formed in a predetermined pattern of conductor traces extending laterally on the thin base to provide “both thin conductors for fine resolution conductors and thick conductor areas for power circuits” on a single layer board (See Pedretti, Paragraph 16).

As also discussed above, the Patel reference does not teach or disclose areas of thick conductive material that are covered by the sublayer. Rather, in the Patel reference, the material only fills the depressed portions, leaving the protuberances of conductive material exposed for contact with further layers of conductive materials.

The Bokisa reference is directed to “a process for preparing multi-layer printed circuit boards and boards made thereby and a process for improving adhesion between copper circuitry and a dielectric layer” (See Bokisa, Col. 1, lines 5-8). The Bokisa reference does not suggest areas of thick conductive material forming a predetermined pattern of conductor traces. Neither does the Bokisa reference suggest areas of thick conductive material that are covered by the sublayer.

Thus, the combination of Patel and Bokisa cannot fairly suggest all elements of Applicants invention as recited in claims 1 and 25. Claims 4 and 9-12 depend upon claim 1 and claims 28-30 and 32-35 depend upon claim 25, and

thus contain every limitation of claims 1 and 25, respectively. Thus, no further comments concerning claims 4, 9-12, 28-30, and 32-35 are deemed necessary herein to be fully responsive to the Office Action dated March 30, 2006.

Applicant's respectfully submit that a prima facie case of obviousness has not been provided. Therefore, reconsideration and withdrawal of the rejection of claims 4, 9-12, 28-30, and 32-35 is respectfully requested.

### **CONCLUSION**

The foregoing is intended to be a complete response to the Office Action dated October 10, 2006. Reconsideration and withdrawal of the rejections is respectfully requested. Should the Examiner have any questions or comments regarding the foregoing, Applicant's attorney would welcome a telephonic interview with the Examiner.

Respectfully submitted,



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